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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,238	10/27/2003	Herman Ma	02-C-106	4334
7590	11/19/2004		EXAMINER	
Lisa K. Jorgenson, Esq. STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006-5039				LE, THONG QUOC
				ART UNIT
				PAPER NUMBER
				2818

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	10/695,238	Applicant(s)	MA, HERMAN
Examiner	Thong Q. Le	Art Unit	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on _____.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-35 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
5) Claim(s) ____ is/are allowed.
6) Claim(s) 1-5,8-13,15-20,22-35 is/are rejected.
7) Claim(s) 6,7,14 and 21 is/are objected to.
8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

1. Claims 1-35 are presented for examination.

Specification

2. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-5,8-13,15-20,22-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi (U.S. Patent No. 6,809,976).

Regarding claims 1, 10,25,32, Ooishi discloses a memory device (Figure 1), comprising:

an array of memory cells arranged in row and columns (Figure 1, 10) , each memory cell comprising a select transistor and an electrically programmable resistive element coupled in series therewith (Figure 2, MC), each column of memory cells being coupled to a bit line (Figure 2, BL), each row of memory cells being coupled to a word line (Figure 2, WL), the select transistor (Figure 2, ATR) in each memory cell having a control terminal coupled to a corresponding word line (Figure 2, MC has control gate ATR coupled to WL);

address circuitry (Figure 1, 20) for receiving an address value and driving a word line corresponding thereto to a voltage level to activate select transistors of memory cells coupled to the word line corresponding to the address value;

a transistor (Figure 2, DS1) coupled between a first bit line and a first reference voltage level (Figure 2, RFG1);

a reference cell (Figure 2, RMC) coupled to the first bit line (Figure 2, RBL1), comprising a select transistor and a resistive element coupled in series therewith (Figure 2, RMC), the reference cell, the transistor and an addressed memory cell in the column of memory cells coupled to the first bit line forming a differential amplifier circuit (Figure 2, 110, Column 11, lines 53-62) ; and

control circuitry (Figure 1, 5) having an output coupled to a control terminal of the transistor for activating the transistor during a memory read operation (Column 11, lines 1-52) .

Regarding claims 2-5,8-9,11-13,15-20,22-24,26-31,33-35, Ooishi discloses wherein the electrically programmable resistive element of each memory cell comprises

a resistive element having a chalcogenide composition (Figure 2. MC), and wherein the control circuitry deactivates the transistor during a memory write operation (Column 11, lines 12-14), and further comprising write drive circuitry (Figure 2, 90) coupled to the first bit line, for placing on the first bit line during a write operation a predetermined voltage level corresponding to a data value, the predetermined voltage level being one of at least two distinct voltage levels (column 9, lines 28-67, Column 10, lines 1-44), and the write drive circuitry selectively places on the first bit line a second predetermined voltage level between a first voltage level corresponding to a first data value and a second voltage level corresponding to a second data value (Column 9, lines 67-Column 10, lines 1-29), and wherein the electrically programmable resistive element in each memory cell is programmable to one of at least two distinct resistance values (Column 11, lines 33-47), and the resistive element in the reference cell has a resistance value between the at least two distinct resistance values (Column 11, lines 33-47), and further comprising a first load element coupled between a second reference voltage level and each memory cell coupled to the first bit line, and a second load element coupled between the second reference voltage level and the reference cell (Figure 2, 102, 106).

Allowable Subject Matter

5. Claims 6-7, 14, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-7, 14,21 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ooishi (U.S. Patent No. 6,809,976), and others, does not teach the claimed invention having wherein the write drive circuitry places the second predetermined voltage level on the first bit line prior to or at the beginning of a memory write operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER